IN THE CLAIMS

1. (Currently Amended) A flat-type capacitor comprising:

a lower interconnection on a predetermined portion of a semiconductor substrate;

a lower electrode that has a flat shape, the lower electrode ~~that is~~ electrically coupled to the lower interconnection, the lower interconnection disposed below the lower electrode;

a concave dielectric layer formed on the lower electrode;

a concave upper electrode formed on the dielectric layer, ~~wherein the concave upper electrode is larger than the lower electrode~~ a bottom part of the concave upper electrode larger than the lower electrode;

a first upper interconnection being electrically coupled to the lower interconnection; and

a second upper interconnection that is coupled to the first upper interconnection.

2. (Original) The capacitor of claim 1, wherein the lower electrode is positioned between edges of the concave upper electrode.

3. (Original) The capacitor of claim 1, wherein the lower electrode and the upper electrode are composed of a material selected from the group consisting of Ti, Ta, W, TiN, TaN, Al, Cu, Ru, Pt, Ir, and combinations thereof.

4. (Currently Amended) The capacitor of claim 1, wherein the dielectric layer is composed of a material selected from the group consisting of SiO_2, Si_3N_4, Ta_2O_5, Al_2O_3, HfO, ZrO_2, ~~BST, PZT, and ST~~ $BaSrTiO_3$, $PbZrTiO_3$, and $SrTiO_3$.

5. (Original) A flat-type capacitor comprising:

a first metal interconnection formed on a predetermined surface of a semiconductor substrate;

a first interlayer dielectric formed on the first metal interconnection and the semiconductor substrate;

a second interlayer dielectric formed on the first interlayer dielectric;

a lower electrode formed on the first interlayer dielectric and coupled to one side of the first metal interconnection;

a second metal interconnection formed on the first interlayer dielectric and electrically isolated from the lower electrode;

a third interlayer dielectric formed on the second interlayer dielectric;

a concave dielectric layer formed on the lower electrode and the second interlayer dielectric;

a concave upper electrode formed along a top surface of the concave dielectric layer, wherein the concave upper electrode is larger than the lower electrode;

a fourth interlayer dielectric formed on the concave dielectric layer, the concave upper electrode, and the third interlayer dielectric; and

a plurality of third metal interconnections formed on the fourth interlayer dielectric, wherein one of the third metal interconnections is coupled to the upper electrode and another one of the third metal interconnections is coupled to the second metal interconnection.

6. (Original) The capacitor of claim 5, wherein the lower electrode is positioned between edges of the concave upper electrode.

7. (Original) The capacitor of claim 5, wherein the upper electrode and the second metal interconnection are formed of the same material.

8. (Original) The capacitor of claim 7, wherein the lower electrode, the second metal interconnection, and the upper electrode comprise material selected from the group consisting of Ti, Ta, W, TiN, TaN, Al, Cu, Ru, Pt, Ir, and combinations thereof.

9. (Original) The capacitor of claim 5, wherein the lower electrode, the second metal interconnection, and the second interlayer dielectric have the same thickness.

10. (Currently Amended) The capacitor of claim 5, wherein the dielectric layer comprises a material selected from the group consisting of SiO_2, Si_3N_4, Ta_2O_5, Al_2O_3, HfO, ZrO_2, ~~BST, PZT, and ST~~ $BaSrTiO_3$, $PbZrTiO_3$, and $SrTiO_3$.

11. (Original) The capacitor of claim 10, wherein the first, second, third, and fourth interlayer dielectrics have the same etch selectivity.

12. (Withdrawn) A method of manufacturing a flat-type capacitor, the method comprising:

forming a lower interconnection on a predetermined portion of a semiconductor substrate;

forming a lower electrode that is electrically coupled to the lower interconnection;

forming an interlayer dielectric over the lower electrode;

forming an etched region by etching the interlayer dielectric until the lower electrode and an area surrounding the lower electrode is exposed;

forming a concave dielectric layer and a concave upper electrode in the etched region of the interlayer dielectric, wherein the concave upper electrode is larger than the lower electrode; and

simultaneously forming a first upper interconnection that is electrically coupled to the lower interconnection, and a second upper interconnection that is electrically coupled to the upper electrode.

13. (Withdrawn) The method of claim 12, wherein forming a lower electrode that is electrically coupled to the lower interconnection comprises:

forming a first insulating layer on the semiconductor substrate and the lower interconnection;

forming at least two plugs in the first insulating layer that are in contact with the lower interconnection, wherein one of the at least two plugs contacts a side of the lower interconnection, and another one of the at least two plugs contacts another side of the lower interconnection; and

forming a second insulating layer on the first insulating layer and the at least two plugs;

forming the lower electrode in the second insulating layer in contact with the one of the at least two plugs; and

forming a metal interconnection in the second insulating layer in contact with the another one of the at least two plugs, wherein the metal interconnection is electrically coupled to the second upper interconnection.

14. (Withdrawn) The method of claim 13, wherein forming the lower electrode in the second insulating layer and forming the metal interconnection in the second insulating layer comprises:

defining a first region where the lower electrode will be formed and a second region where the metal interconnection will be formed by etching the second insulating layer until the at least two plugs are exposed;

depositing a metal layer on the second insulating layer that fills the first and second regions; and

forming the lower electrode and the metal interconnection by planarizing the metal layer until the surface of the second insulating layer is exposed.

15. (Withdrawn) The method of claim 12, wherein forming the concave dielectric layer and the concave upper electrode in the etched region of the interlayer dielectric comprises:

depositing a dielectric layer on the interlayer dielectric and an entire surface of the etched region;

depositing a conductive layer on an entire surface of the dielectric layer; and

polishing the conductive layer and the dielectric layer using a chemical mechanical polishing process until a top surface of the interlayer dielectric is exposed.

16. (Withdrawn) The method of claim 15, further comprising:

forming a buffer oxide layer after depositing the conductive layer but before polishing the conductive layer and the dielectric layer, wherein the buffer oxide layer is removed during the chemical mechanical polishing process.

17. (Withdrawn) The method of claim 12, wherein the lower electrode, the second metal interconnection, and the upper electrode comprise a material selected from the group consisting of Ti, Ta, W, TiN, TaN, Al, Cu, Ru, Pt, Ir, and combinations thereof.

18. (Withdrawn) The method of claim 17, wherein the lower electrode, the second metal interconnection and the upper electrode are deposited at temperatures of about 250° to 500° C.

19. (Withdrawn) The method of claim 18, wherein the lower electrode, the second metal interconnection, and the upper electrode are formed using a process selected from the group consisting of chemical vapor deposition, physical vapor deposition, atomic layer deposition, and electroplating.

20. (Withdrawn) The method of claim 12, wherein the dielectric layer comprises a material selected from the group consisting of SiO_2, Si_3N4, Ta_2O_5, Al_2O_3, HfO, ZrO_2, BST, PZT, and ST.

21. (Withdrawn) A method of manufacturing a flat-type capacitor, the method comprising:

forming a lower metal interconnection on a predetermined portion of a semiconductor substrate;

forming a first interlayer dielectric on the semiconductor substrate and the lower metal interconnection;

forming a first and second plug in the first interlayer dielectric that contact the lower metal interconnection;

forming a second interlayer dielectric on the first interlayer dielectric, the first plug, and the second plug;

forming a lower electrode in contact with the first plug and a middle metal interconnection in contact with the second plug;

forming a third interlayer dielectric on the second interlayer dielectric, the lower electrode, and the middle metal interconnection;

defining a capacitor region by exposing the lower electrode and an area of the second interlayer dielectric that surrounds the lower electrode;

forming a dielectric layer and an upper electrode in the capacitor region, wherein the upper electrode is larger than the lower electrode;

forming a fourth interlayer dielectric on the third interlayer dielectric and the capacitor region;

forming a third plug in the fourth and third interlayer dielectrics that contacts the middle metal interconnection and forming a fourth plug in the fourth interlayer dielectric that contacts the upper electrode; and

forming a first upper metal interconnection that contacts the third plug and a second upper metal interconnection that contacts the fourth plug.

22. (Withdrawn) The method of claim 21, wherein forming the first interlayer dielectric and forming a first and second plug comprise:

depositing a dielectric material on the semiconductor substrate;

forming via holes by etching the first interlayer dielectric until two separate regions of the first metal interconnection are exposed;

depositing a conductive layer on the first dielectric material that fills the via holes; and

planarizing the conductive layer until the first dielectric material is exposed.

23. (Withdrawn) The method of claim 21, wherein forming the second interlayer dielectric, forming the lower electrode, and forming the middle metal interconnection comprise:

depositing a dielectric material on the first interlayer dielectric and the first and second plugs;

forming etched regions by etching the dielectric material until the first plug, the second plug, an area surrounding the first plug, and an area surrounding the second plug are each exposed;

depositing a conductive layer on the dielectric material so as to fill the etched regions; and

planarizing the conductive layer until the dielectric material is exposed.

24. (Withdrawn) The method of claim 21, wherein forming the dielectric layer and the upper electrode comprises:

depositing a dielectric material over an entire surface;

depositing a conductive layer on the dielectric layer; and

polishing the conductive layer and the dielectric layer using a chemical mechanical polishing process until the surface of the third interlayer dielectric is exposed.

25. (Withdrawn) The method of claim 24, further comprising:

forming a buffer oxide layer after depositing the conductive layer but before polishing the conductive layer and the dielectric layer, wherein the buffer layer is removed during the chemical mechanical polishing process.

26. (Withdrawn) The method of claim 21, wherein the lower electrode, the middle metal interconnection and the upper electrode comprise a material selected from the group consisting of Ti, Ta, W, TiN, TaN, Al, Cu, Ru, Pt, Ir, and combinations thereof.

27. (Withdrawn) The method of claim 26, wherein the lower electrode, the middle metal interconnection and the upper electrode are deposited at a temperature of about 250° to 500° C.

28. (Withdrawn) The method of claim 27, wherein the lower electrode, the middle metal interconnection, and the upper electrode are formed using a process selected from the group consisting of chemical vapor deposition, physical vapor deposition, atomic layer deposition, and electroplating.

29. (Withdrawn) The method of claim 21, wherein the dielectric layer comprises a material selected from the group consisting of SiO_2, Si_3N_4, Ta_2O_5, Al_2O_3, HfO, ZrO_2, BST, PZT, and ST.

30. (Withdrawn) The method of claim 21, wherein the first, second, third, and fourth interlayer dielectrics have the same etch selectivity.